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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,845	09/12/2003	Brett W. Murdock	SC13070TH	7050

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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/660,845	MURDOCK ET AL.	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/12/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 20 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 5,7-14,16-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Moyer (US5894562).

4. As to claim 1, Moyer discloses a method for arbitrating for access to a slave device, comprising:

initiating an access to the slave device by a master device; (Moyer teaches in figure 1 of a plurality of masters, CPU1 and CPU2 wanting access to Slave device memory 6, COL. 3, lines 11 - 20)

determining that the access is an undefined length burst access, wherein the undefined length burst access comprises an undefined number of access beats; (Moyer teaches that when a lock signal is asserted, from either master, the current master retains access for an undefined number of cycles, COL. 3, lines 21 – 25)

determining that a predetermined number of access beats of the undefined length burst access will be transmitted between the master device and the slave device before

allowing access to the slave device to be arbitrated; (Moyer teaches of blocking any arbitration for a pre-determined time, COL. 6, lines 9 – 11)

determining that the predetermined number of access beats have occurred during the undefined length burst access; (Moyer teaches in figure 2 of timer 7, with predetermined controls that determines the access time period, COL. 6, lines 11 – 13) and allowing arbitration for access to the slave device only after the predetermined number of access beats. (Moyer teaches that after bus ownership by master device that has been granted the bus access cannot be granted until after the predetermined time, COL. 6, lines 13 – 16).

5. As to claim 2, Moyer discloses The method of claim 1 further comprising correlating the predetermined number of access beats to a value stored in a storage element of a data processing system. (Moyer teaches of completion of the count, thus said correlation, COL. 6, lines 13- 14).

6. As to claims 3, 4,and 8, Moyer discloses the method and circuit, further comprising providing a counter, and arbitrating for access to the slave device is allowed after each time the counter counts the predetermined number of access beats. (Moyer teaches of counter 7 in figure 2, and allowing for an arbitration phase after the counter counts the predetermined number of access beats, COL. 6, lines 11 – 13).

7. As to claim 5, Moyer discloses the method of claim 1, further comprising arbitrating for access to the slave device after the predetermined number of access beats in a modulus manner. (Moyer teaches that arbitrating access to the slave device can be programmed in a modulus fashion, COL. 6, lines 9 – 11).

8. As to claim 7, Moyer discloses an arbitration circuit for arbitrating access to a slave device by a plurality of master devices, the arbitration circuit comprising:

an undefined length burst arbitration circuit, coupled to the slave device and to the plurality of master devices, the undefined length burst arbitration circuit for determining that an access to the slave device is an undefined length burst access, and for allowing arbitration of the slave device only after a predetermined time period during the undefined length burst access; (Moyer teaches of gaining access to a slave device (shared memory 6 of figure 1) with arbitration circuit arbiter 5, providing arbitration between master devices CPU1, and CPU2. Moyer teaches of undefined length burst access when a lock signal is asserted, from either master, the current master retains access for an undefined number of cycles, COL. 3, lines 21 – 25)

and a storage element for storing a value corresponding to the predetermined time period. (Moyer teaches of storage element, control register 20 of figure 6 that stores the predetermined time period, as arbitration will not occur until control bit 22 is cleared. COL. 4, lines 35 – 40)

9. As to claim 9, Moyer discloses the arbitration circuit further comprising a counter coupled to the storage element, the counter for counting the predetermined number of beats, the counter being reloaded after counting the predetermined number of access beats, and wherein arbitration for access to the slave device is allowed only after each time the counter counts the predetermined number of access beats during the undefined length burst access. (Moyer teaches in figure 5 timer 81 comprising counter for counting the predetermined count, COL. 4, lines 21 – 22).

10. As to claim 10, Moyer discloses the arbitration circuit of claim 8 further comprising a counter coupled to the storage element, the counter for counting the predetermined number of beats, wherein arbitration for access to the slave device is allowed on every access beat following the predetermined number of access beats during the undefined length burst access. (Moyer teaches in figure 5 of said counter in timer 81 coupled to control storage element through 27, COL. 4, lines 13 – 21).

11. As to claims 11 - 13, Moyer discloses the arbitration circuit; wherein the predetermined time period corresponds to a predetermined number of system clock cycles during the undefined length burst access. (Moyer teaches of using system clock cycles as the measuring stick, COL. 6, lines 33 – 37).

12. As to claim 14, Moyer discloses the arbitration circuit, wherein the storage element is a bit field portion of a control register. (Moyer teaches of storage element being a part of a storage register in figure 6, COL. 4, lines 35 – 40).

13. As to claim 16, Moyer discloses a method for arbitrating for access to a slave device by a plurality of master devices, comprising: initiating an access to the slave device by a master device of the plurality of master devices; determining that the access is an undefined length burst access, wherein the undefined length burst access comprises an undefined number of access beats; (Moyer teaches of gaining access to a slave device (shared memory 6 of figure 1) with arbitration circuit arbiter 5, providing arbitration between master devices CPU1, and CPU2. Moyer teaches of undefined length burst access when a lock signal is asserted, from either master, the current master retains access for an undefined number of cycles, COL. 3, lines 21 – 25)

loading a counter with a first predetermined value; (Moyer teaches of having predetermined conditions on the timer, COL. 6, lines 11 – 13)

changing a count value of the counter for each access beat until a second predetermined value is reached; (Moyer teaches of software control of the timer which would allow changing the count value for each access beat, COL. 6, lines 9 – 11)

and allowing arbitration of access to the slave device to occur only after the count value is equal to the second predetermined value. (Moyer teaches of software control of the timer, which would allow changing the count value for each access beat, COL. 6, lines 9 – 11).

14. As to claim 17, Moyer discloses the method of claim 16, further comprising reloading the counter with the first predetermined value each time the counter reaches the second predetermined value. (Moyer teaches of software control of the timer, which would allow changing the count value for each access beat, COL. 6, lines 9 – 11).

15. As to claim 18, Moyer discloses the method of claim 16, further comprising reloading the counter with the first predetermined value after mastership of the slave device is lost. (It would have been inherent to have the system on reboot and restoration top have the first predetermined value as the default value).

16. As to claim 20, Moyer discloses the method of claim 19, further comprising implementing the data processing system on an integrated circuit. (Moyer teaches said embodiment in COL. 2, lines 59 – 63).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 6,15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyer as applied to claim1 above, and further in view of Goodwin et al (US6353876) hereinafter Goodwin.

19. As to claims 6, 15,and 19 Moyer does not explicitly disclose the method and apparatus, further comprising implementing the method in a data processing system having a plurality of master ports coupled to a plurality of slave ports via a crossbar switch. (However, Goodwin teaches of a data processing system with a plurality of master ports in figure 1 (CPU0 – CPU3) coupled to a plurality of slave ports M0 – M3 through a cross bar switch. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Moyer and Goodwin as Goodwin needs an arbiter 14 as can be seen from figure 1 to manage access to the shared memory resource, COL. 4, lines 64 – 67).

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAD
6/23/05

TIM VO
PRIMARY EXAMINER